A Dual-Band E-Band Quadrature VCO with Switched Coupled Transformers in 28nm HPM bulk CMOS

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***Abstract* — This paper presents a quadrature VCO (QVCO) that employs gate-to-drain transformers to couple two fundamental oscillators to generate accurate quadrature phases and switched coupled inductors for tuning extension. Thanks to these techniques, it is possible to cover two bands with a single quadrature VCO, without jeopardizing phase noise or demanding extensive silicon area. The oscillator, realized in 28nm HPM bulk CMOS, occupies a core area of only 0.031mm^2 and is tunable from 71-to-76GHz and 85.6-to-90.7GHz, resulting in a total tuning range of 9.8GHz. The peak phase noise at 10MHz offset from the carrier is -117.7dBc/Hz in the lower band and -110dBc/Hz in the higher one and varies less than 3.5dB within each sub-band. The maximum phase error is 1.5° and 3.5° in the lower and higher band respectively.**

***Index Terms* — Quadrature voltage-controlled oscillator (VCO), millimeter-wave, low phase noise, E-Band, CMOS.**

I. Introduction

The atmospheric window from 70-to-100GHz shows attenuation less than 0.5dB/km, and two bands from 71-to-76GHz and 81-to-86GHz (the E-Band) have been allocated for wireless point-to-point communication links. These E-Band communication systems provide a wireless cost-effective multi-Gb/s alternative to fiber optics over short to medium distances.

Furthermore, direct-conversion transceiver architectures with high throughput, low power consumption and low area have been proven in silicon based technologies for 60GHz applications [1]. However, such architectures put stringent requirements on the local oscillator (LO) in terms of tuning range (TR) and phase noise (PN), while demanding quadrature phases at mm-Wave. Addressing these challenges in deep scaled CMOS technology where the degradation of the passives quality factor (Q) at high frequencies is only partially compensated by the increase of the transistor f_t is not trivial [2]. Several recent works have focused on integrated frequency generation circuit in the 70/100GHz bands applying different techniques [3-8] (e.g. frequency multipliers or polyphase filters). However, to cover two bands of 5GHz each separated in frequency with a single low noise CMOS LO solution with quadrature outputs remains an open challenge.

In this paper two fundamental oscillators are coupled by means of gate-to-drain transformers to impose quadrature operation while switched coupled inductors are used to realize tuning extension. Thanks to the proposed techniques the oscillator, realized in 28nm HPM bulk CMOS, occupies a core area of only 0.031mm^2 and is tunable from 71.4-to-76.1GHz and from 85.6-to-90.7GHz, resulting in a total tuning range of 9.8GHz, while achieving state-of-the-art PN performance and providing accurate quadrature phases.

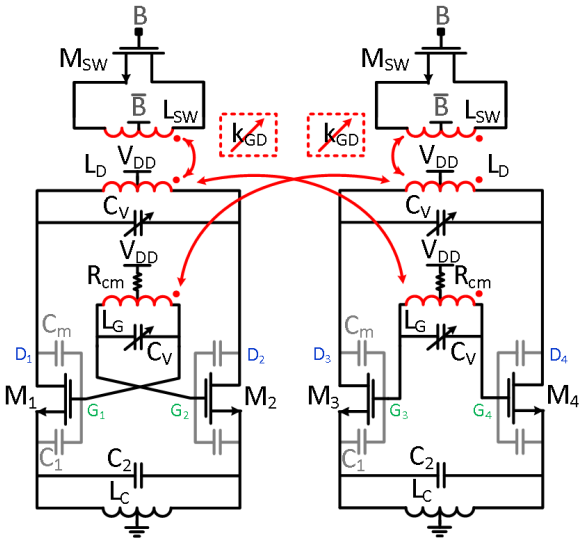

Fig. 1. Schematic of the proposed 28nm transformer coupled Quadrature VCO with switched coupled inductors

II. Proposed Architecture

Fig. 1 shows the schematic of the proposed 28nm quadrature VCO and Fig. 2 the simplified lumped model of the gate-to-drain transformers with switched coupled inductors.

A. Transformer Coupled QVCO Oscillation Frequency

In [8] two oscillators are coupled by means of gate-to-drain transformers leading to low noise performance and low quadrature error over a limited tuning range. To guarantee the start-up conditions, the tank at the source side has to show a capacitive impedance at the designed oscillation frequency (i.e. the resonant frequency of this tank should be lower than f_{osc}). To simplify the analysis, it is therefore beneficial to model it as a capacitor C_2 in

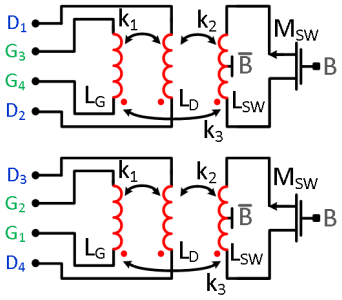

Fig. 2. Simplified lumped element model of the gate-to-drain transformers with switched coupled inductors

parallel with a choke inductor L_c. By inspection, the two possible oscillation frequencies of this oscillator can be written as

$$\omega_{1,2}^2 \approx \omega_0^2 \frac{2+\alpha_1 \pm \sqrt{\alpha_2^2+4+4k_{GD}^2(\alpha_1+\alpha_3)}}{2(1-k_{GD}^2)} \quad (1)$$

where $(\omega_0)^2=1/[L_0C_m(\alpha_1+\alpha_3)]$, $\alpha_1=(C_D+C_G)/C_m$, $\alpha_2=(C_D-C_G)/C_m$, $\alpha_3=C_DC_G/(C_m)^2$, $L_0=L_G/2\approx L_D/2$, $C_D=2C_V$ and $C_G=2C_V+C_1C_2/(C_1+2C_2)$.

When $\omega_{1,2}$ are spaced enough, the transconductors are not able to compensate the tank losses in the higher mode, therefore only one possible stable mode meets the Barkhausen criteria in differential operation. Moreover, R_{cm} is added in the low current bias path of the gate to avoid common mode oscillation, without affecting the performance in differential mode.

B. Proposed Gate-to-Drain Transformer with Switched Coupled Inductors

Design wide tuning range VCOs at mm-Wave is a difficult task if the tuning is realized with a bank of switched capacitors only. Several alternative tuning extension techniques suitable for mm-Wave applications have been proposed in literature, such as [2,4].

A switched-triple-shielded transformer was proposed in [4] to effectively change the equivalent magnetic coupling of a transformer. From (1) it is evident that the same concept can be applied for tuning extension in this topology, where transformers are also used to impose

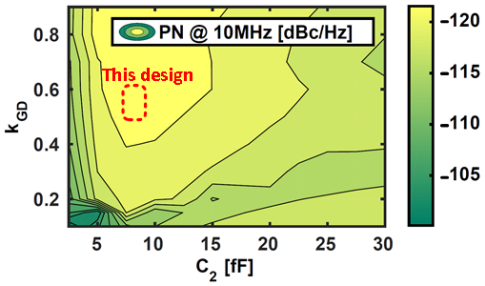

Fig. 3. Simulated phase noise at 10MHz offset from an 80GHz carrier versus k_{GD} and C_2

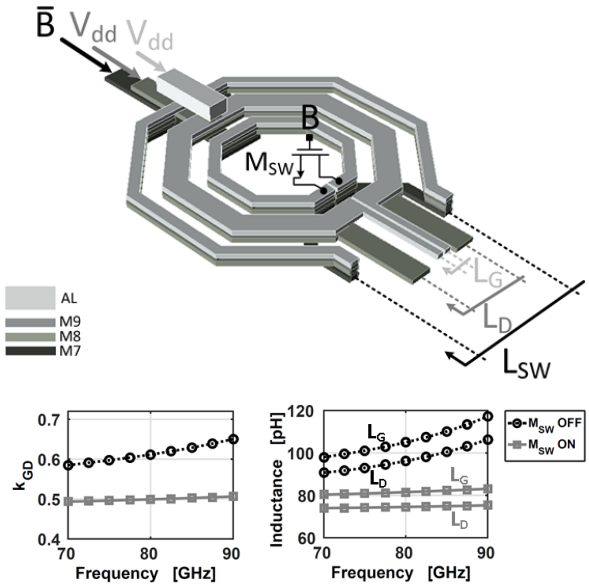

Fig. 4. Proposed gate-to-drain transformer with switched coupled inductors layout and its simulated characteristics

quadrature operation.

To gain more insight, it is useful to refer to the simplified lumped model in Fig. 2. The primary and secondary windings of the transformer (i.e. L_G and L_D) are coupled to each other with a magnetic coupling coefficient k_1. A third winding L_{SW} is also coupled to $L_{G,D}$ through k_2 and k_3. By switching ON and OFF M_{SW}, the current induced in L_{SW} finds a low impedance path or a high impedance one. It is therefore possible to change the effective equivalent magnetic coupling coefficient by acting on k_2 and k_3 [4]

$$k_{GD} = k_1 - k_2k_3 \quad (2)$$

III. Circuit Design

The QVCO was designed and prototyped in TSMC 28nm HPM CMOS technology without RF thick metal option. The core transistors $M_{1,2,3,4}$ are sized up to 40µm/28nm to ensure reliable start-up condition.

In Fig. 3 the simulated phase noise at 10MHz offset from an 80GHz carrier is plotted versus k_{GD} and C_2. Simulations were performed with post-layout parasitics extracted transistors (C_m and C_1 are the parasitic capacitances of $M_{1,2,3,4}$.) and ideal lumped element model for passive components (C_v=10fF, Q=4, V_{dd}=0.7V). Since the proposed topology shows a weak dependency from k_{GD}, magnetic tuning techniques can be adopted as a solution to achieve a wide tuning range without jeopardizing phase noise performance at mm-Wave. Furthermore, C_2 can be designed to reach the phase noise optimum in the higher band (i.e. M_{SW} ON) where the quality factor of the tank is degraded the most, aiming at a uniform noise Figure of Merit over a large tuning range.

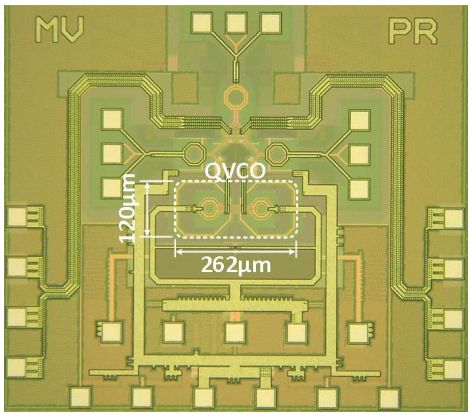

Fig. 5. Die micrograph of the realized test chip (core dimensions: 120µm x 262µm)

The sizing and layout of M_{SW} prove critical, since the parasitic on resistance (R_{on}) and off capacitance (C_{off}) defines the variation in k_{GD} and the tank quality factor [4]. An odd number of fingers is chosen to obtain a symmetric parasitic capacitance at the drain and at the source side. From post layout simulations, M_{SW} has been designed with an aspect ratio of (39 x 3)µm/28nm for an optimal trade-off between C_{off} and R_{on}. Fig. 4 shows the layout and simulated characteristics of the proposed transformer with switched coupled inductors. L_D and L_G are single turn octagonal inductors implemented in M8 and M9 respectively. The metal width is 4µm and the outer diameter is 37.8µm. The outer and inner coils in Fig. 4 are implemented in M8 and M9 and connected together to realize L_{SW}. The metal width is 2µm and the inner spacing from $L_{D,G}$ is 2.9µm whereas the outer spacing is 3.5µm.

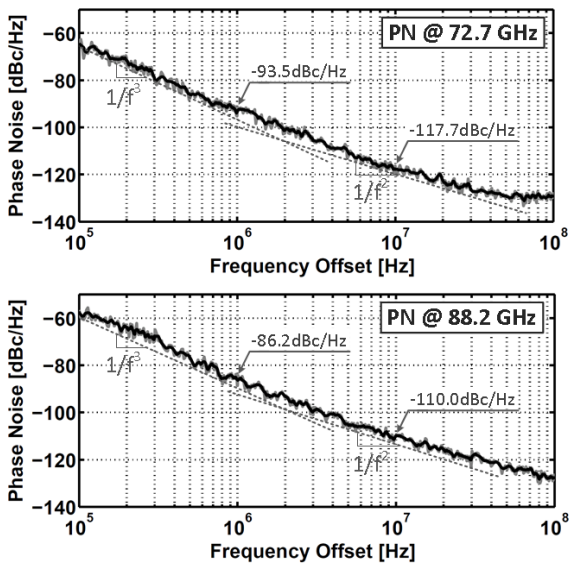

Fig. 6. Measured phase noise from a 72.7GHz carrier and from a 88.2GHz carrier

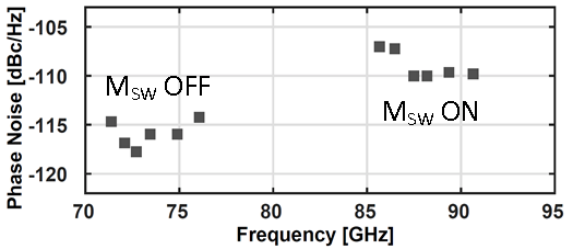

Fig. 7. Measured phase noise across the tuning range

From electromagnetic simulation the equivalent magnetic coupling coefficient, self inductances and quality factors of primary and secondary windings of the transformer when M_{SW} is OFF (ON) are k_{GD}=0.59 (0.5), L_G=100pH (82pH), L_D=92pH (75pH), Q_G=8 (6), Q_D=13 (9) at 73.5GHz (83.5GHz). Noteworthy, the equivalent self inductances of the primary and secondary windings of the transformer vary as well, resulting in a more effective tuning capability.

IV. Experimental Results

Fig. 5 shows the chip micrograph. For testing purpose also two buffers and a double balanced I/Q mixer are implemented on-chip.

The QVCO occupies an active area of 0.031mm^2 and is tunable from 71.4-to-76.1GHz when M_{SW} is OFF and from 85.6-to-90.7GHz when M_{SW} is ON, corresponding to 9.8GHz of total tuning range. 2 binary-weighted digitally controlled capacitors and an A-MOS varactor realize continuous tuning within the two bands. The control voltage of varactors is varied between 0-1.2V. The availability of digital transistor models only resulted in a shift of the upper band by 4.6GHz toward higher frequencies, also giving rise to a deviation from the optimal point and a degradation of noise performance in this band.

Fig. 6 shows the phase noise at 72.7GHz and 88.2GHz, measured after downconverting the mm-Wave signal at the output of the buffer with an external mixer. The 1/f^3 corner is ~2MHz and phase noise at 1MHz and 10MHz offset are -93.5dBc/Hz and -117.7dBc/Hz from a 72.7GHz carrier and -86.2dBc/Hz and -110dBc/Hz from a 88.2GHz carrier. Fig. 7 shows the measured phase noise at 10MHz offset versus the oscillation frequency. The QVCO dissipates 35.6mW from a 0.7V supply and the phase noise ranges from -114.2 to -117.7dBc/Hz in the lower band and from -107 to -110dBc/Hz in the higher band, yielding to a FOM that ranges from 176.3 to 179.4dBc/Hz and from 170.2 to 173.4dBc/Hz respectively. I/Q imbalance is measured by applying an external tone to the on-chip quadrature mixer driven by the presented QVCO and measuring the IF outputs with a sampling oscilloscope. Fig. 8 shows a screenshot of the oscilloscope with the I/Q signals downconverted to 260MHz. The measured phase

TABLE I

COMPARISON WITH STATE-OF-THE-ART INTEGRATED FREQUENCY GENERATION CIRCUITS IN 70/100GHZ BAND, WITHOUT QUADRATURE PHASES (TOP) AND PROVIDING I/Q SIGNALS (BOTTOM)

Ref.	Topology	Freq. (GHz)	TR (GHz)	Power (mW)	PN @10MHz (dBc/Hz)	FOM @10MHz (dBc/Hz)	Phase Error	Area (mm^2)	Tech.
[3]	40GHz VCO + Freq. Doubler	73.9-83.5	9.6	227	-111/-113.2	165.8/167.1	**NO** I/Q OUTPUT	n.a.	130nm SiGe
[4]	Fund.VCO	57.5-90.1	32.6	8.4/10.8	-104.6/-112.2	172/180	**NO** I/Q OUTPUT	0.03	65nm CMOS
[5] VCO1	Fund.VCO	73.1-78.7	5.6	12	-109.4	176.2	**NO** I/Q OUTPUT	0.013*	65nm CMOS
[5] VCO2	Fund.VCO	87.1-91.7	4	11	-108.3	176.9	**NO** I/Q OUTPUT	0.013*	65nm CMOS
[6]	Fund.VCO + RC PPF	70-89	19	310.2	-107/-114#	159/168.1	< 8.5°	0.107+	0.35µm SiGe
[7]	25GHz VCO + Freq. Tripler	70.5-85.5	15	47.3	-108.3/-111.7#	170.1/172.2	< 2°	0.291+	65nm CMOS
[8]	Fund.QVCO	83.7-88.7	5	28.4	-108.5/-118.8	172.5/183.2	< 1.2°	0.030	40nm CMOS
This Work	**Fund.QVCO**	**71.4-76.1 85.6-90.7**	**9.8**	**35.6**	**-114.2/-117.7 -107/-110**	**176.3/179.4 170.2/173.4**	**< 1.5° < 3.5°**	**0.031**	**28nm CMOS**

Estimated from the reported phase noise @1MHz offset * VCO core + buffer + Graphically estimated

error is less than 1.5° in the lower band and less the 3.5° in the higher one, while the amplitude error is less than 1dB over the whole tuning range.

The measured quadrature VCO performance is summarized and compared with state-of-the-art integrated frequency generation circuits in 70/100GHz bands with and without I/Q outputs in Table I. Noteworthy, solutions based on polyphase filter (PPF) [6] and frequency multipliers [7] dissipate about 60% of the power in the buffer driving the filter and 50% in the tripler respectively, leading to a low noise FOM while consuming large silicon area.

V. CONCLUSION

Thanks to the presented design techniques, the 0.031mm^2 28nm CMOS oscillator prototype achieves state-of-the-art phase noise performance over two bands of about 5GHz each separated in frequency, without trading in silicon area.

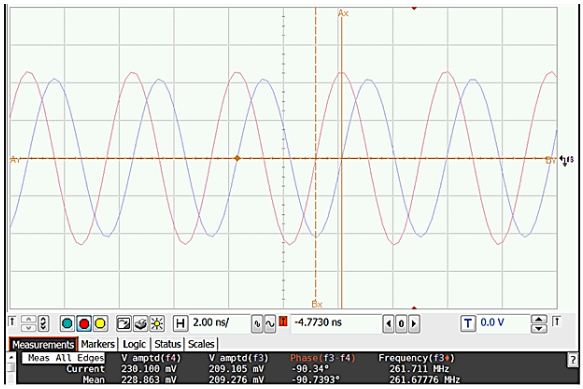

Fig. 8. Measured phase and amplitude imbalance of the I/Q signals downconverted to 260MHz

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